

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

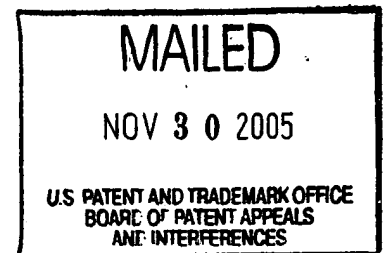
UNITED STATES PATENT AND TRADEMARK OFFICE

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Ex parte PIERRE GAUTIER AND THOMAS LEDRU

Appeal No. 2005-2683
Application No. 09/808192

ON BRIEF



Before KRASS, GROSS, and BLANKENSHIP, Administrative Patent Judges.
KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1, 2, 5/2/1, 5/1, 6, and 7.

The invention pertains to variable bit rate video encoders, best illustrated by reference to independent claim 1, reproduced as follows:

1. A variable bitrate video encoding method comprising, for encoding a sequence of frames, at least a quantization step of an input bitstream, a coding step of said quantized bitstream, and a control step of the quantization step with respect to a buffer occupancy at the output of said coding step, said method being characterized in that it also comprises an analysis step, for defining a reserve of bits (ROBC) indicating a

number of bits used for coding each frame is either greater or less than a predetermined number, and an additional control step, for maintaining, increasing or decreasing the quantization step value according to the state of said reserve of bits.

The examiner relies on the following reference:

Odaka et al. (Odaka)	5,317,397	May 31, 1994
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Claims 1, 2, 5/2/1, 5/1, 6, and 7 stand rejected under 35 U.S.C. § 102 (b) as anticipated by Odaka.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

A claim is anticipated only when a single prior art reference expressly or inherently discloses each and every element or step thereof. Constant v. Advanced Micro-Devices Inc., 848 F.2d 1560, 1570, 7 USPQ2d 1057, 1064 (Fed. Cir. 1988); RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984). If the examiner presents a reasonable basis for alleging inherency, the burden shifts to appellants to come forward, if they can, with evidence to the contrary. In re King, 801 F.2d 1324, 1327, 231 USPQ 136, 138 (Fed. Cir. 1986); In re

Ludtke, 441 F.2d 660, 664, 169 USPQ 563, 566-67 (CCPA 1971); In re Swinehart, 439 F.2d 210, 213, 169 USPQ 226, 229 (CCPA 1971).

The examiner's position in reading Odaka on the instant claims is set forth at pages 3-6 of the answer.

Appellants' position is that Odaka only discloses setting the ratios of the quantization step size according to Equation 3 (column 23 of Odaka), and, at column 23, lines 30-34, that an amount of bits allocated to each picture is determined to satisfy certain conditions in accordance with rules (I) and (II) (set forth at lines 34-51 of column 23 of Odaka), and does not disclose "defining a reserve of bits (ROBC) indicating a number of bits used for coding each frame is either greater or less than a predetermined number," as required by the instant claims [see pages 4-5 of the principal brief].

In response to the examiner's rebuttal, at pages 6-7 of the answer, wherein the examiner points to Odaka's column 24, lines 39-50, for a teaching of an allocation of bits and a determination of whether that amount exceeds a predetermined percentage, and where the examiner points to Odaka's column 22, lines 48-57, and column 23, lines 9-45, for a teaching of a rate control technique and an updating of the number of

allocated bits needed to encode a picture, appellants argue, at pages 2-3 of the reply brief, that Odaka does not anticipate “maintaining, increasing or decreasing the quantization step value according to the state of said reserve of bits,” as recited in claim 1. Appellants further state that Odaka does not disclose that the quantization step size Q is incremented or decremented according to the amount of bits allocated. Instead, contend appellants, Odaka bases the increment or decrement on a buffer threshold and buffer occupied amount of the previous slice. Therefore, conclude appellants, it cannot be reasonably said that Odaka discloses “maintaining, increasing or decreasing the quantization step value according to the state of said reserve of bits,” as required by the claims.

We have carefully reviewed the evidence before us, including the Odaka reference and the arguments of appellants and the examiner, and we conclude therefrom that the examiner has established a prima facie case of anticipation which has not been successfully rebutted by appellants. Accordingly, we will sustain the rejection of claims 1, 2, 5/2/1, 5/1, 6, and 7 under 35 U.S.C. § 102 (b).

Following the examiner’s reasoning, at pages 3-6 of the answer, the examiner specifically points to particular portions of Odaka corresponding to each of the claimed steps. In particular, the examiner identifies portions of Odaka wherein an “excess or

shortage of the amount of bits..." (Column 23, lines 13 et seq.) is recited. There is an update of the "allocated amount of bits" (Column 24, line 39) of a picture. A quantization step is incremented/decremented according to the state of the bits in a buffer (Column 28, lines 6-14).

Yet, in the face of the reasonable conclusions reached by the examiner from Odaka's disclosure, and without specifically pointing out how the examiner's rationale is perceived to be in error, appellants merely argue that since Odaka "only discloses setting the ratios of the quantization step size according to Equation 3," Odaka "does not disclose 'defining a reserve of bits (ROBC) indicating a number of bits used for coding each frame is greater or less than a predetermined number', as required by the claim" (principal brief-page 4). Such an "argument" fails to show any error in the examiner's reliance on columns 22-23 of Odaka for the teaching of defining a reserve of bits indicating the number of bits used for coding each frame is greater or less than a predetermined number.

In discussing column 23, lines 30-34, of Odaka, at pages 4-5 of the principal brief, appellants merely allege, without explanation, that Odaka "only discloses an amount of bits allocated to each picture is determined to satisfy...the above described conditions according with the following rules (I) and (II)" and that "it is evident" that

Odaka fails to disclose “defining a reserve of bits (ROBC) indicating a number of bits used for coding each frame is either greater or less than a predetermined number.” It is unclear as to why appellants conclude that Odaka’s disclosure makes it “evident” that there is no disclosure therein of “defining a reserve of bits (ROBC) indicating a number of bits used for coding each frame is either greater or less than a predetermined number,” especially in the face of the examiner’s reasonable explanation as to how Odaka may be interpreted to, in fact, disclose “defining a reserve of bits (ROBC) indicating a number of bits used for coding each frame is either greater or less than a predetermined number.” Accordingly, appellants have not convinced us of any error in the examiner’s position.

Similarly, in the reply brief, appellants contend that “it is evident” that Odaka does not disclose that quantization step size Q is incremented or decremented according to the amount of bits allocated disclosed in column 23. Instead, argue appellants, the increment/decrement is based on a BT (buffer threshold) and buffer occupied amount of the previous slice. Therefore, conclude appellants, it is not reasonable to interpret Odaka as disclosing “maintaining, increasing or decreasing the quantization step value according to the state of said reserve of bits” (reply brief-page 3).

We are unconvinced by appellants' argument. It is true, from column 28, lines 6-15, of Odaka, that a buffer occupied amount is monitored in units of slices, and that if the buffer occupied amount is larger or smaller than a threshold value and is larger or smaller than the buffer occupied amount of the previous slice, a quantization step size Q is incremented by one or decremented by one. However, it appears from column 26, lines 29 et seq. of Odaka, that quantization step sizes of the slices of the buffer are obtained on the basis of an allocated amount of bits and an activity (see, for example, column 26, lines 29-32). Thus, it would appear, contrary to appellants' position, that Odaka does disclose "maintaining, increasing or decreasing the quantization step value according to the state of said reserve of bits." Appellants' argument appears to rest on only one portion of the Odaka disclosure but fails to take into account how that portion (e.g., the "buffer" disclosure at column 28, lines 6-14) of the disclosure is tied to the rest of the disclosure (e.g., Column 26, lines 29-36, of Odaka) wherein the slices of the buffer are related to the allocated amount of bits.

We do not say that there is no argument that appellants could have made convincing us of no anticipation of the instant claims by the Odaka disclosure. We merely assert that if there is, appellants have simply not made it. Accordingly, since all of appellants arguments have been answered and no such argument convinces us of any error in the examiner's rationale for the rejection of the instant claims, the

examiner's decision rejecting claims 1, 2, 5/2/1, 5/1, 6, and 7 under 35 U.S.C. § 102 (b)
is affirmed.

No time period for taking any subsequent action in connection with this appeal
may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED



ERROL A. KRASS
Administrative Patent Judge



ANITA PELLMAN GROSS
Administrative Patent Judge



HOWARD B. BLANKENSHIP
Administrative Patent Judge

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